Multi-I/O and Reconfigurable RF/Wireless Interconnect Based on Near Field Capacitive Coupling and Multiple Access Techniques

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Abstract

Future ULSI interconnect system demands extremely high data transmission rate, multi-I/O service, reconfigurable and fault-tolerant computing/processing architecture and full compatibility with mainstream silicon CMOS and MCM technologies. In this paper, we present a novel RF/wireless interconnect system that provides a unique solution to those system needs. Unlike the traditional "passive" metal interconnect, the "active" RF/wireless interconnect is based on near-field capacitive coupling, low loss and dispersion-free microwave signal transmission and modern multiple-access algorithms. The proposed RF/wireless interconnect promises ultra-broad bandwidth (up to **100GHz**), simultaneous multi-I/O communications (up to **50/50 I/O sub-channels** per shared microwave transmission medium) and reconfigurable network (programmable based on **F**requency and/or **C**ode **D**ivision **M**ultiple **A**ccess). As the first step to prove the feasibility, we have realized a **2x2 CDMA transceivers** based on 0.35μm MOSIS CMOS process, which demonstrates the desired functions of capacitive coupling, guided wave transmission and reconfigurable multiple access.

Introduction

As illustrated in Fig.1, the RF/wireless interconnect system may be described as a miniature wireless LAN located inside a MCM package. Like any other wireless systems, this miniature LAN contains ULSI I/Os as users, capacitive couplers as near field antennas, RF transceivers and an off-chip but in-package MTL (microstrip transmission line) as a shared broadcasting medium. Output signals can be up-linked to MTL via transmission capacitive couplers (C_T), then down-linked via receiving capacitive couplers (C_R) to input ports to fulfill the interconnect function. With a shared MTL, modern code division (**CDMA**) and/or frequency division (**FDMA**) multiple-access algorithms can be used to alleviate the cross-channel interference. With orthogonal-coded and/or frequency-filtered RF transceivers, a passive MTL is suitable to relay ultra-broadband signals up to 100GHz [1].

RF/Wireless Interconnect System

Figure 2 shows a representative RF interconnect channel shared by multiple I/Os. Since the channel is designed to hold bi-directional communications, both ends of the MTL are terminated with Z_C to avoid the signal reflection. The I/O impedance of the transceivers (Tx and Rx) is ranged in kilo-Ω while the C_R and C_t are estimated to be 1000μm^2 in size and 25μm apart from the MTL. With those designs, EM full-wave analysis suggests that low loss and dispersion-free transmission over a broadband (100GHz) may be achievable with signal-to-noise budget as calculated in Fig.3 for reaching a low bit-error-rate (BER) $<10^{-14}$. Where the system is designed to hold 25 carrier-channels and each carrier-channel covers 4GHz band and containing 4 CDMA sub-channels with 1 Gbps/sub-channel.

CDMA Transceiver Demonstration

We have successfully demonstrated an on-chip 2x2 CMDA RF-interconnect system with 0.35μm CMOS. As shown in Figs.4 and 5, the demo chip contains two sets of transceivers (Tx and Rx), T/R capacitive couplers, a shared transmission medium, high impedance source-follower front-ends, analog to digital converts and a reconfiguration enable switch. In each Tx, input data is spread by orthogonal-Walsh codes and then coupled into the shared medium through T/R couplers. In each receiver, transmitted data is first quantized by ADC and then despread by a CDMA correlator. Reconfiguration enable is implemented for data path selection between two channels. Fig. 6 shows the test results of channel reconfiguration at 4MHz (6(a)) and 200MHz (6(b)), respectively. The maximum clock rate of the designed RF-interconnect is about 500MHz with power consumption of 50mW/transceiver. Presently, we are designing a next generation 2GHz CDMA transceiver based on 0.18μm CMOS. The power consumption of this chip will be reduced to 21mW/transceiver. The speed-power consumption relationship for future RF-interconnect implementation is estimated in TABLE-I according to the CMOS scaling rule of $P \propto f V_{dd}^{\ 2} C_L$ and the forecasted minimum power supply voltages and clock rates by SIA's ITRS road map (1997).

Table-I

Year	1999	2002	2005	2008	2011	2014
CMOS Process (μm)	0.18	0.13	0.10	0.07	0.05	0.035
ITRS min Clock rate (GHz)	1.25	2.1	3.5	6.0	10.0	13.5
Estimated Clock rate (GHz)	2.0	3.3	>5	>9	>15	>20
ITRS max. V_{dd} (V)	1.8	1.5	1.2	0.9	0.6	0.6
ITRS min. V_{dd}(V)	1.5	1.2	0.9	0.6	0.5	0.3
Power Consumption/ Transceiver (mw)	10~21	8~20	4~18	3~15	2~12	1~10

Reference

[1] Computer Aided Design of Microwave Circuits (1981), by K.C. Gupta et al., Artech House.

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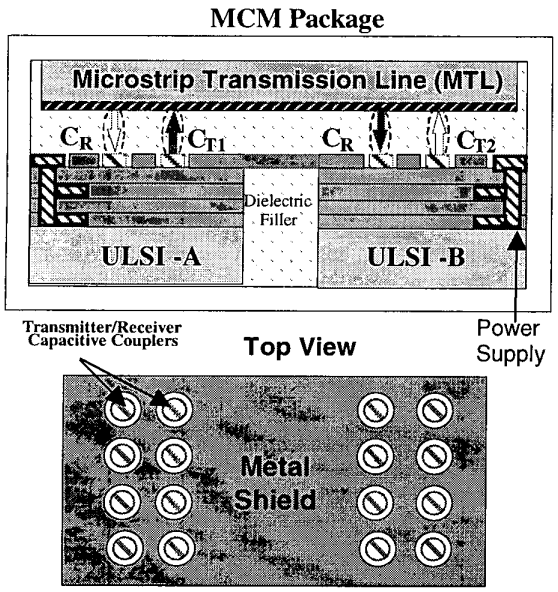

Fig.1 RF/wireless interconnect for inter- and intra-chip communications

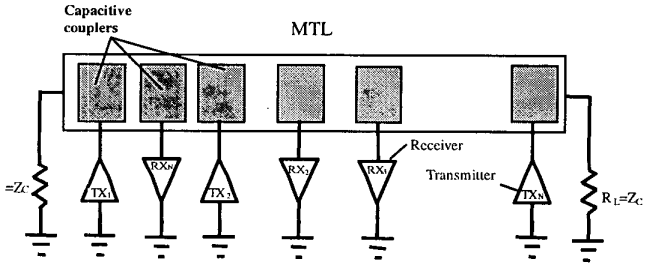

Fig.2 Multiple I/Os share a common MTL with characteristic impedance Z_c

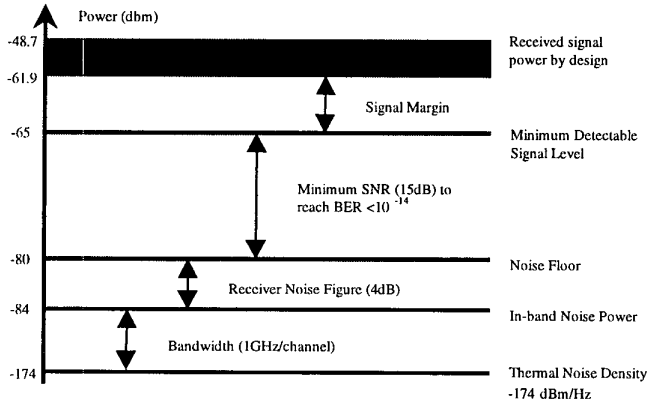

Fig.3 Signal-to-noise budget for RF/Wireless Interconnect system

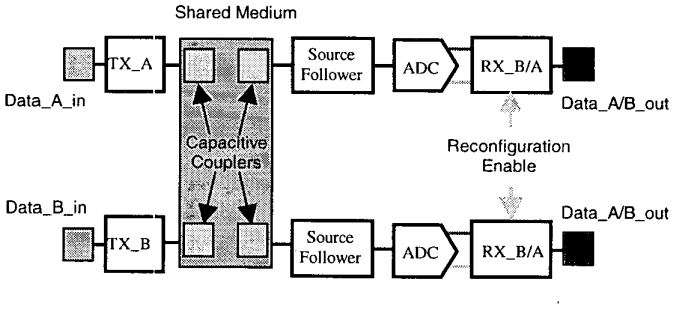

Fig.4 2x2 CDMA RF/wireless interconnect system

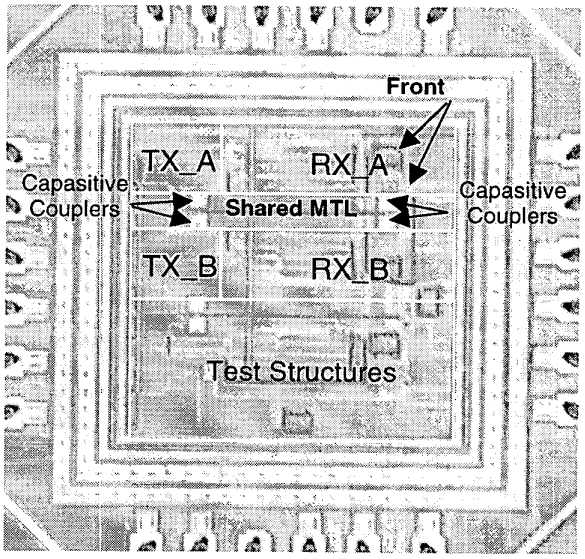

Fig.5 Fabricated CMOS 2x2 RF/Wireless interconnect

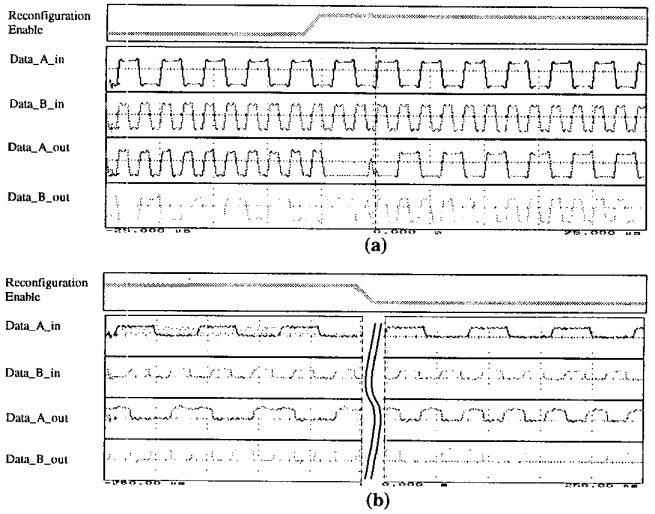

Fig.6 Channel reconfiguration demonstrated at (a) 4MHz, and (b) 200MHz clock rates (speed limited by MOSIS package)