

# **Synopsis: Preventive circuitry**

April 25, 2011

In transistor circuits, preventing logical errors with physical fault tolerance is more efficient than correcting errors with a fault-tolerant architecture.



Credit: Sami Mitra

The electronics industry's access to smarter, lighter, and more powerful devices depends on whether transistor circuits—the building blocks of such devices—can process large amounts of information. As circuits get faster and smaller, errors—arising from heat dissipation, noise, and structural disorder—in the physical information they process can impede development. Experts debate on whether to concentrate on inherent physical fault tolerance that prevents error generation, or on architectural fault tolerance that corrects errors by sophisticated algorithms.

Writing in *Physical Review Letters*, Thomas Szkopek at McGill University, Canada, and colleagues in the US quantify these error-suppressing processes for model nanoelectronic systems. Using the electron number as the dimensionless size parameter for logic gates, they estimate the minimum number of electrons necessary for reliable circuit logic. They find that the physical fault tolerance in transistor circuits suppresses the error rate per electron number exponentially, compared to only subexponential suppression of error rate in the most efficient fault-tolerant architecture of logical gates. Their conclusion—that error prevention is better than error correction—has implications for transistor device technologies and CMOS scaling, and may impose a minimum limit on the size of devices. – *Manolis Antonoyiannakis* 

#### **Physical Fault Tolerance of Nanoelectronics**

Thomas Szkopek, Vwani P. Roychowdhury, Dimitri A. Antoniadis, and John N. Damoulakis Phys. Rev. Lett. 106, 176801 (2011) Published April 25, 2011

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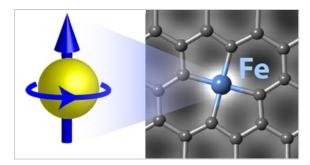
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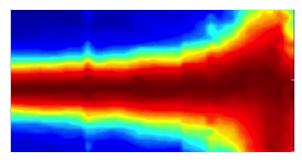


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